NED UNIVERSITY OF ENGINEERING & TECHNOLOGY, KARACHI
FINAL YEAR (COMPUTER SCIENCE AND INFORMATION TECHNOLOGY)
ANNUAL EXAMINATION 2007
BATCH 2003-04

Time: 3 Hours **Dated: 04-10-2007**
Max. Marks: 80

PARALLEL PROCESSING – (CS-451)

Instructions:
1. Attempt any five questions. All questions carry equal marks.
2. Questions may be attempted in any order, but all parts of the same question must be together.
3. Give short and precise answers.
4. Make logical assumptions where necessary.

Q1 a The goal of parallel processing is to solve problems faster at any cost. Comment. 1

b What is a grand challenge? Give an example. 2

c Can parallelism be achieved in EREW PRAM? If yes, how? If no, why not? 2

d Consider the algorithm given below and trace through it for 16 processors. What is the space complexity of this algorithm? What is the time complexity of this algorithm? 7

```
Algo Broadcast_EREW
Processor P1
        y(in P1's private memory)←x
        L[1]←y
for i=0 to (log2 p)-1 do
        forall Pj, where 2^i+1≤j≤2^(i+1) do in parallel
                y(in Pj's private memory)←L[j-2^i]
                L[j]←y
        endfor
endfor
```

e What do you mean by cost of a parallel algorithm? What is a cost optimal parallel algorithm? 2

f For a parallel algorithm, $T(n)=3\log n^3+(\log n)^2$. $P(n)=\log n^4$. What is its cost? 2

Q2 a Name the appropriate class from Flynn's taxonomy and draw a representative diagram, that: 4
   i. Resembles pipeline stages,
   ii. Incorporates maximum parallelism.

b Explain directory protocols for cache coherence. 4

c What do you mean by safe and unsafe periods for a data piece? 2

d Consider a multiprocessor system using MESI protocol for cache coherence. It has 3 processors: A, B, and C. The table shows states of various blocks in the three caches. 6

Block	C_A	C_B	C_c
x		M	
y			E

The following events occur in order:
   i. A asks for block x to read.
   ii. B asks for block y to write.

For each event:
- Indicate who makes read miss/hit, write miss/hit, snoop read/write hit, and
- Explain the transitions.

Q3 a In dataflow architecture, what do you mean by: 2
   i. Firing of a node,
   ii. Ready cell?
   b Draw a diagram of the Manchester Dataflow Machine. Was it static or dynamic architecture? Explain its working. 7
   c Route a message from node 29 to node 100 in a 7-cube. 5
   d Give formulae for bisection bandwidth of a mesh of mxn. 2

Q4 a What are the Bernstein's conditions? How are they of use to us? 4
   b Which kind of dependence is machine specific? Explain it with example. 3
   c What is latency of an interconnection network? What are its components? Explain them. Which of them are program dependent? Why do you say so? 7
   d For an interconnection network, define: 2
   i. Concurrency,
   ii. Scalability.

Q5 a How was parallelism achieved in CDC-6600? Draw the diagram of its CPU. 3
   b Explain memory interleaving with proper diagram. 3
   c Name the four levels of parallelism. 2
   d Draw an 8X8 Benes network recursively, showing all steps. Derive a formula for the number of switches in an NXN Benes network. How many switches are used if N=8? 6
   e Show β_2 connections for 16 nodes. 2

Q6 a Differentiate between 4
   i. Unifunctional and multifunctional pipelines,
   ii. Linear and nonlinear pipelines.
   b For the given reservation table, show: 4
   i. Collision vector,
   ii. Greedy cycles,
   iii. Upper and lower bounds on MAL.
   iv. The revised table after delay insertion.

	0	1	2	3
S1	X			X
S2		X	X	
S3	X		X	X

   c Draw a crossbar. Is it a non-blocking or a blocking network? What is its diameter? How many switches are needed in an NXN crossbar? What is its disadvantage? 5
   d Draw and name the different possible states in which an exchange element can be set in a multistage interconnection network. 2
   e An Omega network is better than a crossbar. Comment. 1

Q7 a For the following set of instructions, show the data dependences and the final order of execution. 10
   S1: A=Y^2
   S2: B=Z^2
   S3: C=Y-B
   S4: D=Z-A
   S5: A=A-B
   S6: C=C*D
   S7: C=C/A
   b The message passing architecture is a multiprocessor architecture. Do you agree? Give reason. 2

c What do you mean by memory collisions? If I connect all memory modules and all processors to a ring, such that: 4

i. A processor grabs a token to access memory,
ii. A processor releases a token when it receives data from memory, and
iii. A single token is circulated in the ring at the start.

Can memory collisions occur? Why, or why not? Is this shared or distributed memory architecture?

Q8 a For the given reservation table, show: 9

i. Simple cycles,
ii. Greedy cycles,
iii. MAL,
iv. Upper and lower bounds on MAL,
v. Throughput of the pipeline if clock period is 0.02 seconds.

	0	1	2	3	4	5	6	7
S1	X					X		
S2		X	X					
S3	X							X
S4				X	X			
S5		X					X	

b Draw a dataflow diagram for the following piece of code, when x, y and z are input variables (readily available): 7

```
a=pow(z,2);
b=3*x;
b=a-b;
c=pow(x,2);
d=a*c;
d=d+y;
d=b*d;
e=pow(y,2);
f=c*e;
f=f+z;
g=3*e;
g=c+g;
g=f+g;
g=d/g;
```

--GOOD LUCK--